Claim 1				
Spec, inventive embodiments	Hsu et al (6,911,690 B2)	Prior Art as Admitted by Applicant	Sakui et al (6,411,548 B1)	
NAND flash memory cell array	Y (Figs. 1, col. 4, l. 55 -col. 6, l. 24)	Y (Fig.1 + discussion of Background + p.4, l.1-2)	Y (e.g., Figures 20, 31, 49, col. 16,l.48+)	
substrate with active area	Y (Figs. 1, col. 4, l. 55 -col. 6, l. 24): 100, 104	Y (idem: regs. 26, 24))	Y (e.g., Figures 20, 31, 49, col. 16,l.48+) (regions 21/22, 23)	
bitline diffusion BLD	Y, called "drain region" 124 (e.g., col. 5, l. 7)	Y (bitline diffusion 22, F.1)	Y (e.g., "n-type diffusion layer" 28d in Figure 31; col. 61, l.9)	
source region	Y, called "source region" 126 (e.g., col. 5, l. 7)	Y (element 23 in Fig. 1)	Y (e.g., "n-type diffusion layer 28s in Figure 31; col. 61, l. 9)	
plurality of stacked gates	Y (control gates 120 and floating gates 118) (c.5, l.26+)	Y (control gates 28, floating gates 27; F.1)	N (has control gates but charge storage 26 are insulating gates)	
plurality of select gates	Y (select gates 106; Fig. 1 (c.5, l. 1, e.g.))	Y (29 and 31; see F.1 and p. 2, l. 8+)	Y (27 SSL; F.31 and see c. 7, l. 34 for "SSL")	
last select gate overlaps source	N; hence not 102 over Hsu et al, as admitted.	Y (select gate 31 overlaps source 23 in Figure 1).	Y ("a" 27 transistor as shown in Fig. 49, with gate overlapping 28	Motivation: Chapman (6,118,161), col. 4, l. 21-28, for low resistance/high
bitline BL above row	not shown but inherent in NAND Flash Memory	Y (Fig. 1: horizontal portion or extension of 32)	Y (BL 36 in Fig. 31, e.g.)	Evidence: Matas et al, on Flash Memory Technology (Fig. 10-8)
bitline contact connects BL-BLD	not shown but inherent in NAND Flash Memory	Y (Fig. 1: vertical portion or extension of 32)	Y (31d, Fig. 31)	Evidence: Matas et al, on Flash Memory Technology (Fig. 10-8)
Claim 15				
select gate directly above source			vertical line exists intersecting source and select gate (F.31,49)	
Claim 19				
rows (plural)	Y: see F. 1A and discussion.			
Claim 24				
self-aligned sides	Y (Fig. 1B; see also col. 5, l. 12+ and 27+).			Note: "self-"aligned is a product by process limitation
erase paths	Y (col. 8, l. 61+)			
voltage coupling	Y (voltage coupling inherent			

APPENDIX: TABLE 1.